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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,484	07/20/2006	Philippe Avian	0563-1078	4666

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YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
GETACHEW, ABIY	
ART UNIT	PAPER NUMBER
2841	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,484	AVIAN, PHILIPPE	
	Examiner	Art Unit	
	Abiy Getachew	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/20/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tran et al. (US 20040001533 A1)

Regarding claim 1 Tran et al. discloses a method for optimizing the number of power outputs of an electronic control device (See figure 1 element 112) of the application specific integrated circuit type (120) mounted onto a printed circuit board (Figure 1), the number of power outputs required depending on the application, characterized in that it consists in mounting into two packages (126,128) having geometrically identical connecting configurations, an integrated circuit of a first type comprising a first number of power outputs and an integrated circuit of a second type comprising a second number of power outputs, respectively, in such a manner as to make said two circuits compatible for their installation on the printed circuit board (See figure 1), and to provide at least two locations on the board for the installation of said two packages (126,128), the number of power outputs (123) required for the application being obtained by installing in said locations at least two circuits chosen from between said integrated circuit of the first type (120) and said integrated circuit of the second type (122).

Regarding claim 2 as applied claim 1 above Tran et al. discloses, characterized in that the integrated circuit of the first type (See figure 1) and the integrated circuit of the second type (122) are designed to have a difference of two outputs (123 and 124).

Regarding claim 3 as applied claims 1 and 2 above Tran et al. discloses, characterized in that the integrated circuits (120) of the first type and of the second type are encapsulated within a package of the PQFN type.

Regarding claim 4 as applied claims 1 and 3 above Tran et al. discloses, characterized in that the integrated circuits (120) of the first type (120) and of the second type (122) are encapsulated within a package of the QFN type. (See figure 4)

Regarding claim 5 Tran et al. discloses An electronic control device (See figure 1 element 112) of the application specific integrated circuit type (120) mounted onto a printed circuit board (Figure 1), said device comprising a stage (105,107) with power outputs whose number depends on the application targeted, characterized in that said power output stage comprises at least two circuits over which the required number of power outputs is distributed, said two circuits being chosen from a set comprising an integrated circuit of a first type comprising a first number of power outputs and an integrated circuit of a second type comprising a second number of power outputs, said circuits of the first and of the second type being respectively mounted into two packages (126,128) having geometrically identical connection configurations, in such a manner as to make said two circuits compatible for their installation on the printed circuit board (See figure 1).

Regarding claim 6 as applied claims 5 above Tran et al. discloses, characterized

in that the integrated circuit (120) of the first type comprises six power outputs. (See claim 38, i.e. modification module comprising a first modification module input coupled to the first input, a second modification module input coupled to the second output, and a modification module output to provide the first binary representation of the first digital signal based on a first plurality noise states)

Regarding claim 7 as applied claims 5 and 6 above Tran et al. discloses, characterized in that the integrated circuit (120) of the second type comprises eight power outputs (105,107).

Regarding claim 8 as applied claims 5 and 7 above Tran et al. discloses, characterized in that the integrated circuit (120) of the first type comprises one eight-amp output three three- amp outputs and two one-amp outputs. (See figure 1)

Regarding claim 9 as applied claims 5 and 8 above Tran et al. discloses, characterized in that the integrated circuit (120) of the second type (128) comprises one eight-amp output, four three- amp outputs and three one-amp outputs. [See section 0031, i.e. the receiver power spreading modules 120 and 122 will implement an identical power spreading function. Therefore, for purposes of illustration, only one of the receiver power spreading modules]

Citation of Relevant Art

Irwin et al. (2006/0279038 A1) teaches an electronic display and a card interface adapted to receive a game card having data that represents a particular game outcome such that connection of the card to the interface can result the game being played by the device with the particular outcome displayed on the display.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abiy Getachew whose telephone number is (571) 272 6932. The examiner can normally be reached on Monday to Friday 8Am to 4:30Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abiy Getachew
Examiner
Art Unit 2841

A.G.
August 14, 2007

DEAN A. REICHARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

8/20/07